



**HARDWARE  
REFERENCE DESIGN**

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# **UM670A-03**

**Automotive-grade Multi-Constellation  
Dual-Frequency GNSS Navigation and  
Positioning Module**

# Revision History

Version	Revision History	Date
R1.0	First release	Dec., 2023



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# Foreword

This document describes the hardware reference design of Unicore UM670A-03 module.

This is only a draft version, for reference only.

## Target Readers

This document applies to technicians who are familiar with GNSS receivers.

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# 1 Block Diagram

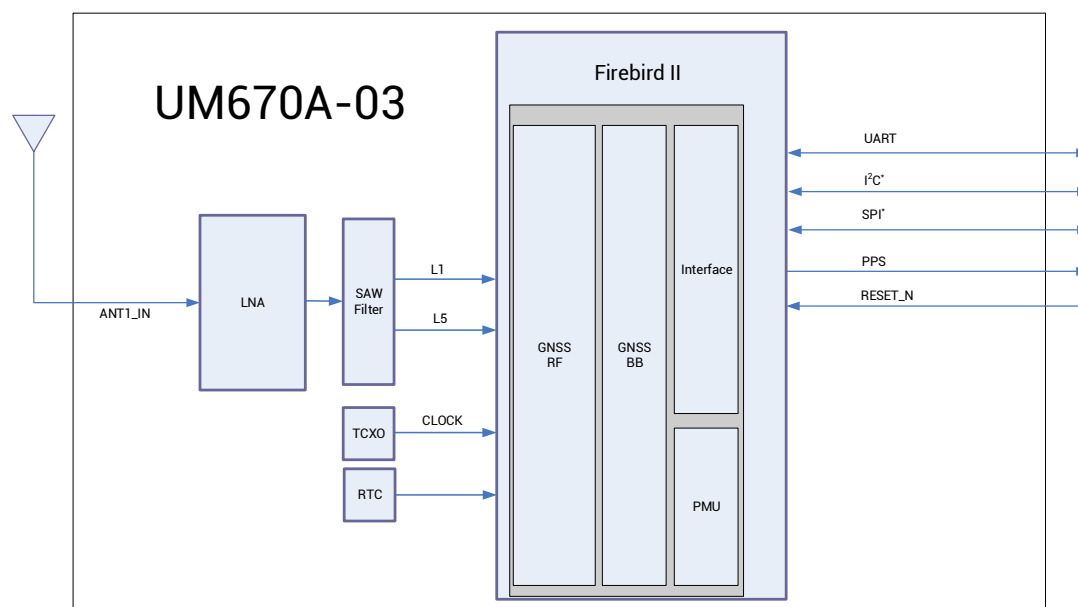
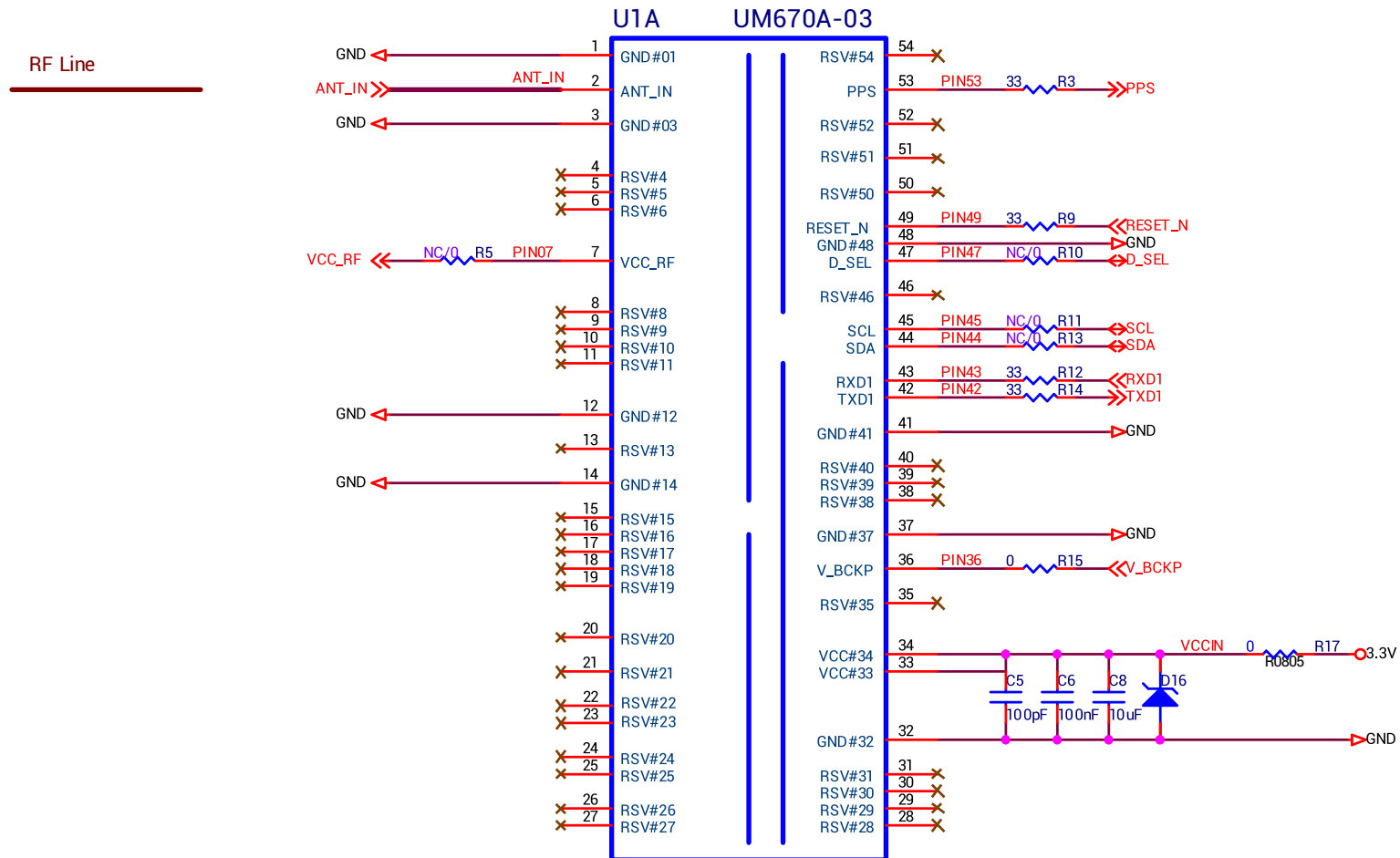


Figure 1-1 UM670A-03 Block Diagram\*

## 2 UM670A-03 Peripheral Design

- Connect the ANT\_IN signal to the antenna, and note the 50  $\Omega$  impedance matching.
- Connect all the GND pins to the ground.
- Leave the IO pin open if not used
- Recommended to add TVS anti-surge protection at the input of the module. Add ESD protection at all the used pins.

\* I<sup>2</sup>C and SPI are reserved interfaces



**UM670A-03 Module** Note: PINs leave OPEN if not used

Figure 2-1 UM670A-03 Peripheral Design

## UM670A-03 Hardware Reference Design

The GND pads at the bottom of the module should be grounded to ensure heat dissipation.

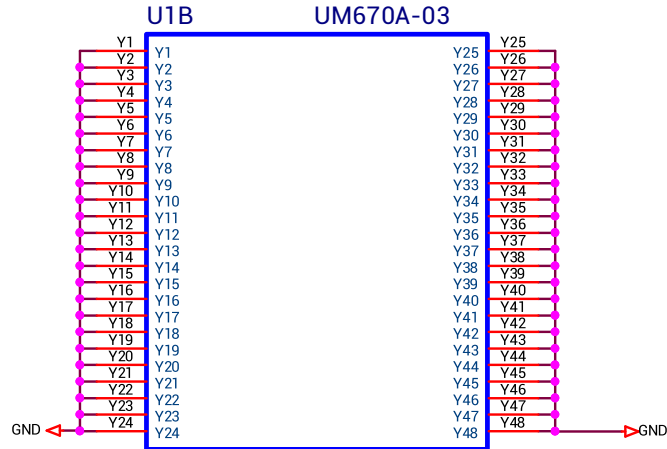


Figure 2-2 UM670A-03 GND Pads

### 2.1 Main Power VCC

The working voltage range of the module UM670A-03 is 2.7 V to 3.6 V.

**Note:**

- The VCC initial level when power-on should be less than 0.4 V.
- The VCC ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% must be within 100  $\mu$ s to 10 ms.
- Power-on time interval: The time interval between the power-off ( $VCC < 0.4$  V) to the next power-on must be larger than 500 ms.



## 2.2 Backup Battery V\_BCKP

When using the hot start function of the module UM670A-03, you need to provide backup power for the module. The input range of V\_BCKP is 1.7 V to 3.6 V.

**Note:**

- The V\_BCKP initial level when power-on should be less than 0.4 V.
- The V\_BCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% V\_BCKP.
- V\_BCKP power-on waveform: The time interval from 10% rising to 90% must be within 100  $\mu$ s to 10 ms.
- Power-on time interval: The time interval between the power-off (V\_BCKP < 0.4 V) to the next power-on must be larger than 500 ms.
- When you do not use the hot start function, connect V\_BCKP to VCC or a standalone power source. Do not connect it to ground or leave it floating.

### 2.3 Active Antenna Feed Circuit

The antenna feed circuit consists of the anti-surge design, filter inductors, and ESD protection. The ESD protection diode should support high-frequency signals (above 2000 MHz).

- It is not recommended to use VCC\_RF to feed the antenna, as it is not optimized for the anti-lightning strike and anti-surge due to the compact size of the module.
- If the antenna feed supply ANT\_BIAS and the module's main supply VCC use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on VCC, which may cause damage to the module. Therefore, it is recommended to design an independent power rail for the ANT\_BIAS to reduce the possibility of module damage.

Connect the ANT\_IN signal to the antenna, and note a 50  $\Omega$  impedance matching.

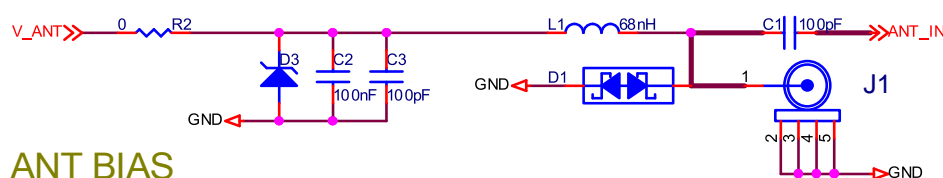
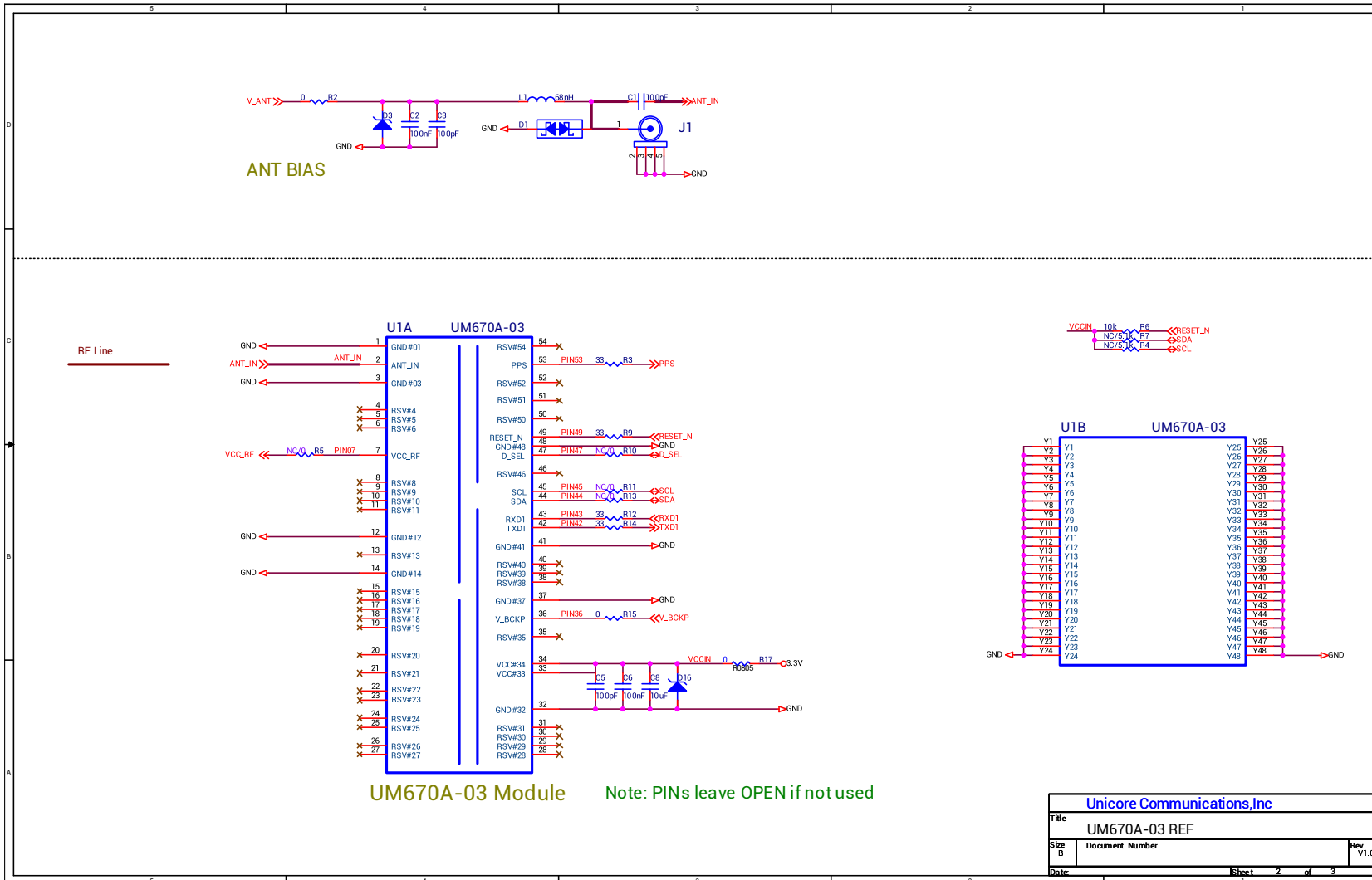


Figure 2-3 Antenna Feed Circuit

### 2.4 Reset Circuit

UM670A-03 supports system reset. The pin RESET\_N is active low and the active time should be no less than 5 ms.

## 3 Appendix: Schematics of Reference Design



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